IN THE CLAIMS

Please amend claims 1-9, and add claims 10-20 as follows:

1.(Currently Amended) A parallel data processing device comprising:

a sensor array for obtaining a signal,

an array of parallel processing elements ~~(LPA1...320)~~ for processing ~~a signal~~ the signal to obtain parallel streams of data, and

means ~~(TSMM1...80)~~ for shuffling the parallel streams of data in a block-wise manner,

wherein a number of columns of the sensor array corresponding to different colors are shared by a same processing element of said array of parallel processing elements.

2.(Currently Amended) ~~A device~~ The parallel data processing device as claimed in claim 1,

wherein the data shuffling means ~~(TSMM1...80)~~ comprise an array of addressable switch memory matrices ~~(TSMM1...80)~~ which are each coupled to a predetermined number of said processing elements

~~(LPA1...320)~~.

3.(Currently Amended) ~~A device~~ The parallel data processing device as claimed in claim 2, wherein each switch memory matrix ~~(TSMM1...80)~~ comprises:

a matrix of registers ~~(MR)~~; and

a crossbar switch having row-wise buses ~~(r1...4)~~ and column-wise buses ~~(c1...4)~~, crossings of the row-wise buses ~~(r1...4)~~ and the column-wise buses ~~(c1...4)~~ being provided with switches ~~(T)~~, each register ~~(MR)~~ being coupled to one row-wise bus ~~(r1...4)~~ and one column-wise bus ~~(c1...4)~~ of the crossbar switch, and each column-wise bus ~~(c1...4)~~ being coupled to a processing element of said array of parallel processing elements ~~(LPA1...320)~~.

4.(Currently Amended) ~~A device~~ The parallel data processing device as claimed in claim 2,

wherein each switch memory matrix ~~(TSMM1...80)~~ is a square matrix.

5.(Currently Amended) ~~A device~~ The parallel data processing

device as claimed in claim 2,

wherein the switch memory matrices ~~(TSMM1...80)~~ are coupled two by two to each other.

6.(Currently Amended) ~~A device~~ The parallel data processing device as claimed in claim 2,

wherein each processing element ~~(LPA1...320)~~ comprises an accumulator ~~(ACC1...320)~~, the accumulators ~~ACC(1...320)~~ of the predetermined number of processing elements ~~(LPA1...320)~~ being selectively addressable.

7.(Currently Amended) ~~Camera~~ A camera system comprising:

~~a sensor array (S) for obtaining a signal; and~~

~~a parallel~~ the parallel data processing device as claimed in claim 1 for processing the signal.

8.(Currently Amended) ~~A camera~~ The camera system as claimed in claim 7

wherein the sensor array ~~(S)~~ is provided with a color filter array~~, and a number of columns of the sensor array (S)~~

~~corresponding to different colors (R,G,B) are shared by a same processing element (LPA1...320)~~.

9.(Currently Amended) A method of processing a signal, comprising the ~~steps~~ acts of:

obtaining the signal using a sensor array;

processing the signal in ~~an array~~ a processing array of processing elements ~~(LPA1...320)~~ to obtain parallel streams of data, and

shuffling ~~(TSMM1...80)~~ the streams of data in a block-wise manner,

wherein a number of columns of the sensor array corresponding to different colors are shared by a same processing element of said processing array.

10.(New) The parallel data processing device as claimed in claim 1,

wherein the sensor array is provided with a color filter array; and wherein said number of columns that are shared by said same processor depends on said color filter array.

11.(New) The parallel data processing device as claimed in claim 1,

wherein the sensor array is provided with a color filter array; and wherein said number of columns that are shared by said same processor depends on a color number of different colors in a row of said color filter array.

12.(New) A processing device comprising:

a sensor array for obtaining a signal,

a processor array of parallel processors for processing the signal to obtain parallel streams of data, and

a shuffler configured to shuffle the parallel streams of data in a block-wise manner,

wherein a number of columns of the sensor array corresponding to different colors are shared by a same processor of said processor array.

13.(New) The processing device as claimed in claim 12, wherein the sensor array is provided with a color filter array; and wherein said number of columns that are shared by said same

processor depends on said color filter array.

14.(New) The processing device as claimed in claim 12, wherein said number of columns is two when said color filter array includes two different colors in a row; and said number of columns is three when said color filter array includes three different colors in a row.

15.(New) The processing device as claimed in claim 12, wherein the sensor array is provided with a color filter array; and wherein said number of columns that are shared by said same processor depends on a color number of different colors in a row of said color filter array.

16.(New) The processing device as claimed in claim 12, wherein the shuffler comprises an array of addressable switch memory matrices which are each coupled to a predetermined number of said processors.

17.(New) The processing device as claimed in claim 16,

wherein each switch memory matrix comprises:

a matrix of registers; and

a crossbar switch having row-wise buses and column-wise buses, crossings of the row-wise buses and the column-wise buses being provided with switches, each register being coupled to one row-wise bus and one column-wise bus of the crossbar switch, and each column-wise bus being coupled to a processor of said processor array.

18.(New) The processing device as claimed in claim 16, wherein each switch memory matrix is a square matrix.

19.(New) The processing device as claimed in claim 16, wherein the switch memory matrices are coupled two by two to each other.

20.(New) The processing device as claimed in claim 16, wherein each processor of said processor array comprises an accumulator, the accumulators of the predetermined number of processing elements being selectively addressable.